

Intelligent Movement and Feedback Controller

FEATURES

- Fully integrated motor-pot controller
- Touch detection and action
- Position recall functionality
- Haptic feedback support
- Programmable force feedback modes
- Programmable tactile feedback events
- Motor thermal profiling and protection
- 3.0 to 5.5V logic voltage range
- 4.5 to 16V motor voltage range
- QWIIC compatible

APPLICATIONS

- Re-configurable input devices
- Haptic feedback for robots
- Educational systems
- Audio mixing consoles
- Broadcast mixing consoles

for PSM Series Motorized Slide Potentiometer

DESCRIPTION

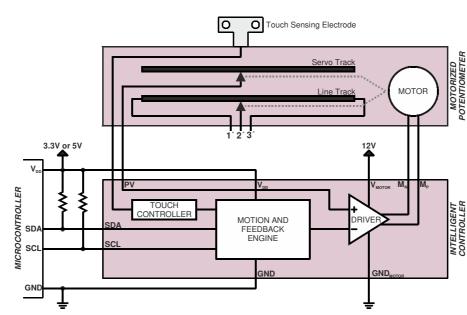
DSPSM1602 is an intelligent controller for motorized potentiometers that will attach as a shield to a Bourns PSM01 or PSM60 motorized potentiometer and provides the functionality necessary to read and drive the potentiometer from any I²C capable microcontroller.

This controller will allow digital read-out of the potentiometer setting as well as motorized recall of positions.

In addition it is possible to trigger tactile feedback events such as vibration as well as configuring force feedback modes such as a center detent, or multiple detents for enumerated inputs.

It is also possible to implement haptic feedback for robotics applications, enabling the user to "feel" the forces applied on the robotic actuator.

The controller contains a touch detector, motion profile generator, PID controller, motor driver and logic, providing a fast and easy path from specification to implementation.





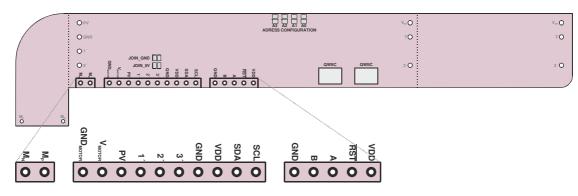
TYPICAL APPLICATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	
V _{DD} to GND	5.5 V
V _{MOTOR} to GND _{MOTOR}	16 V
Ground Potential	
GND to GND _{MOTOR}	±100 mV

Motor Current (Continuous)	1000 mA
Temperature Range40°C	to 85°C
Storage Temperature Range65°C	to 125°C

PIN CONFIGURATION



V _{DD}	Digital Supply Voltage. Typically 3.3V or 5.0V.	1′	Connected to <i>Line Track</i> near end-point. Uncommitted, can be used freely by external
GND	System Ground. Typically tied to GND _{MOTOR} .		circuitry.
V _{MOTOR}	Motor Supply Voltage. Typically 12V	2′	Connected to <i>Line Track</i> wiper. Uncommitted, can be used freely by external circuitry.
GND _{MOTOR}	Motor Ground. Typically tied to GND.	3′	Connected to <i>Line Track</i> far end-point. Uncommitted,
SCL	Connect to I ² C master SCL, requires external pull-up		can be used freely by external circuitry.
	on the I ² C bus.		Active low reset input for the motion and feedback
SDA	Connect to I ² C master SDA, requires external pull-up on the I ² C bus.		engine. Has an on-board pull-up resistor and is typically not connected.
PV	Connected to Servo Track wiper. Typically not connected, but may be connected to a high	M _P , M _N	Motor outputs. Typically not connected.
	impedance input, for example an operational amplifier or an ADC.	А, В	Used for firmware programming and reserved for future application. Do not connect.

Note: The headers marked **QWIIC** will each accept one JST 4-pin connector for easy prototyping and daisy-chaining. When connected to a QWIIC-enabled microcontroller the only other connections required are V_{MOTOR} and GND_{MOTOR} . Please look online for more information on the QWIIC connect system.



ELECTRICAL SPECIFICATION

Parameter	Min	Тур	Max	Unit	Conditions
DIGITAL SUPPLY					-
Supply Voltage (VDD)	3.0	3.3/5.0	5.5	V	
Supply Current (IDD)		16mA	50	mA	
MOTOR SUPPLY					
Motor Voltage (V _{MOTOR})	4.5	12	16	V	
Motor Current (I _{мотов})			500	mA	
Motor Standby Current		0	1	mA	Motor off
LOGIC LEVELS					
Logic High Output (V он)	$V_{DD} - 0.8$			V	
Logic Low Output (VoL)			0.8	V	
Logic High Input (V _{ін})	$0.7 \times V_{DD}$			V	
Logic Low Input (VIL)			$0.30 \times V_{DD}$	V	
					-
ANALOG					
PV impedance	0		10	kΩ	10kΩ servo track, position dependent

PERFORMANCE SPECIFICATION

Parameter	Min	Тур	Max	Unit	Conditions
Digital Readout Resolution			12	bits	
Digital Readout SNR		1		bits	PV_FILTER >= 3, motor standby
Movement Command Error		0.5	2	% full scale	V 10) (factory configuration
Full Range Movement		250	300	ms	$\mathbf{V}_{MOTOR} = 12V$, factory configuration
PWM frequency		100		kHz	
Control loop bandwidth		25		kHz	
PID controller bandwidth		1		kHz	
Motion controller bandwidth		250		Hz	



CONFIGURATION JUMPERS

ADRESS SELECTION (AO...A3)

The I²C slave address of the device is selected by configuring solder jumpers *A0*, *A1*, *A2* and *A3*.

The pads can be soldered together, but will also accept a 0603 component such as a 0-ohm resistor.

A3 is used to select an address range and will in addition to being left open or being bridged, also accept a 5% resistor for extended addressing options.

A2-A0 are used to select an address within that range.

The following tables describe the configuration of A0-A3:

	A3	Range	A2	A1	A0	Address
1	open	16	open	open	open	0
	bridged	24	open	open	bridged	1
	6.8k	32	open	bridged	open	2
	15k	40	open	bridged	bridged	3
	27k	48	bridged	open	open	4
	47k	56	bridged	open	bridged	5
	82k	64	bridged	bridged	open	6
	150k	72	bridged	bridged	bridged	7
	330k	80				

The I²C slave address is the sum of *Range* and *Address*.

Example: A3 is loaded with 27k, A2 and A1 are left open, A0 is bridged. The configured $\ell^{c}C$ slave address is 48+1 = 49.

By default, all jumpers are open and the default address is 16.

GROUND SEPARATION (JOIN_GND)

Joins motor ground (GND_{MOTOR}) and digital ground (GND) together.

This solder jumper is bridged by default.

For applications where it is necessary to separate motor ground from digital ground (e.g. to reduce interference) it is possible to cut this jumper.

GND_{MOTOR} and **GND** <u>must still be tied together</u>, but by cutting this jumper is is possible to externally tie them together using, for example, a ferrite.

For applications that require low-side current sensing for the motor, it is possible to use a small external resistor between GND_{MOTOR} and system ground.

The pads can be soldered together, but will also accept a 0603 component such as a ferrite or a 0-ohm resistor.

POWER SEPARATION (JOIN_SV)

This solder jumper is open/not bridged by default.

For testing, prototyping or specific applications is may be useful to tie digital power (V_{DD}) together with motor power (V_{MOTOR}).

This allows the entire device (controller & motor) to run from a single power connection (e.g. a single QWIIC connector Note1), although the motor will be operating at reduced strength.

This configuration is only supported when 4.5V < V_DD < 5.5V.

The pads can be soldered together, but will also accept a 0603 component such as a ferrite or a 0-ohm resistor.

^{e1} Since QWIIC is 3.3V only, this configuration does not adhere to the QWIIC standard. For full QWIIC compatibility, external power must be supplied to V_{Мотов}

ASSEMBLY INSTRUCTIONS

BOARD AND POTENTIOMETER

If you've purchased the controller and potentiometer separately, you will need to install the potentiometer onto the circuit board.

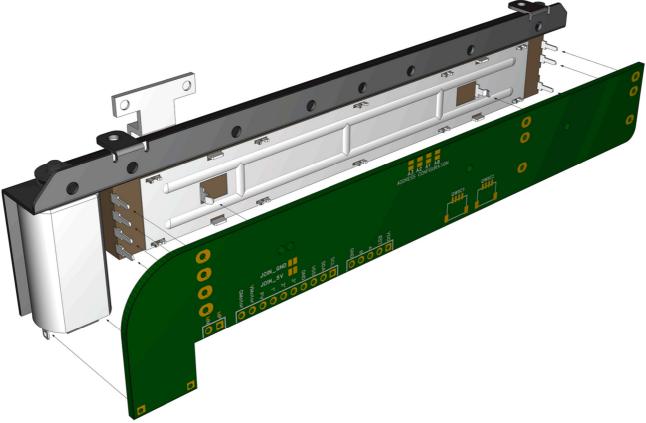
Carefully insert the potentiometer into the circuit board in the orientation shown in the illustration below. A 100mm potentiometer is shown for reference, but the board will accept either a 60mm or 100mm potentiometer.

Make sure the potentiometer firmly inserted and flush before soldering all connections. It is important to also solder the two chassis connections, as these are necessary for proper shielding and function of the touch interface and add additional mechanical support.

You will then need to solder a wire or pin header between each motor lead and its accompanying motor pad, located on the part of the board that extends downwards by the motor.

The black arrows in the illustration below shows all solder connections that need to be made (11 in total).

If you are using a potentiometer with 60mm travel, you should now carefully cut or break off the part of the circuit board that extends beyond the length of this potentiometer. The board has a scoring line marked with the text *PSM60 BREAK LINE*, showing where the board should be detached.



HEADERS

Once you've installed the board, you will likely want to solder a connector to the board.

For most applications it is only necessary to install the middle 10-pin connector, as all other pins are reserved or for special applications only. All connector pads have a standard 2.54mm(0.1") pitch and you can use any compatible header that fits your application.

We typically recommend an angled male pin-header unless your application has special requirements.

If you wish to use the QWIIC system to connect the board to a microcontroller or daisy chain multiple devices, now is a good time to install the QWIIC JST connectors. Please make sure to properly solder the chassis leads on each side of the connector, to ensure that the connector does not break off and damage the board.



SERIAL INTERFACE

OVERVIEW

The DSMP1602 operates only as a slave device on the l²C bus. Connections to the bus are made via the open-drain I/O lines **SDA** and **SCL**. External pull-up resistors must be employed on the bus. DSMP1601 support the transmission protocol for *fast* (up to 400kHz) modes.

To access the DSMP1602, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The DSMP1602 features four address pins (A0 - A4) for address selection, see the **ADDRESS SELECTION** section for more information on available addresses and their configuration.

READING/WRITING

Accessing a particular register on the DSMP1602 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after initiating a write operation. Every write operation to the DSMP1602 requires a value for the pointer register to be transferred.

During a write operation, all following bytes will be written to the register determined by the pointer register.

When reading from the DSMP1602, the last value stored in the pointer register from a write operation will be used to determine which register is read. To change the pointer register for a read operation, a new value must be written to the pointer register. This is accomplished by issuing a write operation, followed by the pointer register byte and no additional data. The master can then issue a read operation to read the specified register.

POINTER REGISTER

Typically, the pointer register will automatically increment after each successful register read or write. This allows reading or

writing of consecutive registers without the need to issue a write operation and pointer register byte for each register.

Some registers however, termed streaming registers, will not increment the register pointer after a successful read or write.

Since each write operation requires a pointer register byte to be sent first, multiple registers can only be written in a single I²C transaction.

For read operations the register pointer will be maintained between transactions and it is possible to read multiple consecutive registers over multiple transactions.

When automatically incrementing the pointer register into a range of non-existing register addresses, the pointer register will automatically skip to the next valid register address.

However, if the pointer register is written with a non-existing register address, it will be reset to 0.

16-BIT REGISTERS

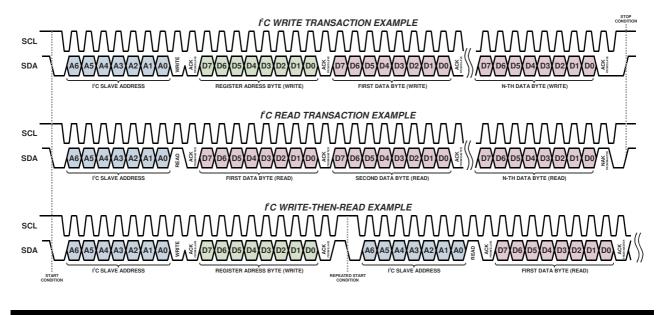
The DSMP1602 contains several 16-bit register that requires special care when reading and writing.

16-bit data is always transferred **BIG ENDIAN** (most significant byte first), also known as network order.

When reading a 16-bit register, always read the most significant byte (MSB) first. The DSMP1602 will latch the least significant byte of the register into a temporary storage when this occurs. When reading the least significant byte (LSB) no actual register access is performed, instead the temporary storage is returned. This prevents incorrect data transfers if the register contents change in between the time of reading the MSB and reading the LSB.

Similarly, when writing a 16-bit register, always write the MSB first. When this occurs no actual register access takes place, instead the MSB will be latched into a temporary storage. When the LSB is written, the MSB from the temporary storage and LSB will be used to write the full 16-bit register.

When reading or writing 16-bit registers always access the MSB and LSB together, in direct succession. These two reads or writes may be split over multiple transactions, but no other registers should be accessed between the two. Doing so invokes undefined behavior.

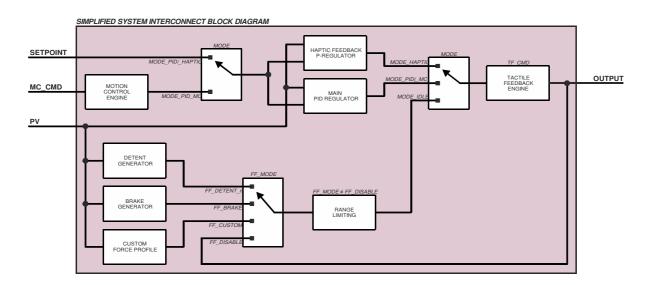


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FUNCTIONAL DESCRIPTION

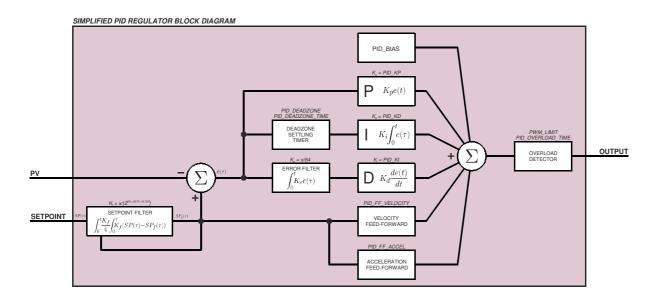
SYSTEM INTERCONNECT

The DSPSM1602 consists of a number of separate and interconnected modules that operate in conjunction with each other to perform all of the tasks related to movement and various feedback modes. The system interconnect fabric is illustrated by the following diagram.



MAIN PID REGULATOR

The DSPSM1602 main regulator is a typical PID regulator with the addition of bias and feed-forward terms, as well as filters specific to accurately regulating and controlling a system based on analog feedback from a potentiometer track. The functionality of the regulator is illustrated by the following diagram.





PROGRAMMING FORCE FEEDBACK MODES

DETENTS

Programming detents consists of two parts - programming detent shape, and programming detent placement.

Detent shape is defined by a deadzone (**FF_DET_DZ**) – the size of the "valley" at the bottom of each detent, the length of the inclines surrounding each detent (**FF_DET_LEN**) and the slope of those inclines (**FF_DET_SLOPE**). In addition, the force feedback mode (**FF_MODE**) defines whether the valleys roll off softly (**FF_DETENT_SOFT**) or sharply (**FF_DETENT_SHARP**). If the values of **FF_DET_DZ** and **FF_DET_LEN** add upp to less than 80h a flat region will be present between the detents, as illustrated in *Example 1*. In *Example 2*, this is not the case – and the peak has no flat region. Detent placement is specified by a scale (**FF_DET_SCALE**) and an offset (**FF_DET_OFFSET**). In *Example 1* scale is defined for 8

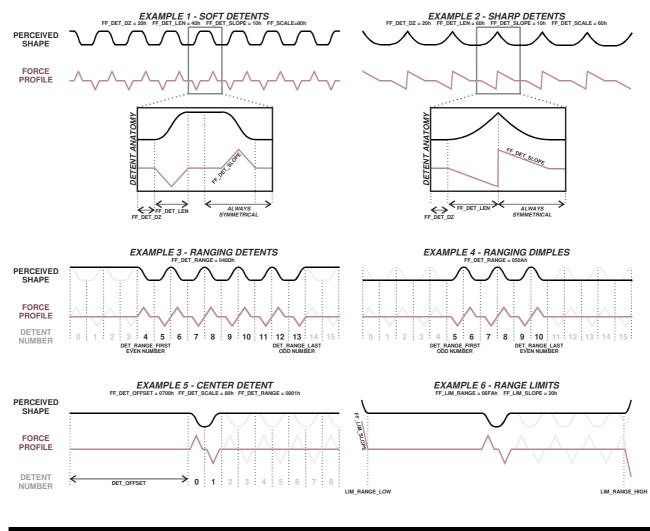
Detent placement is specified by a scale (**FF_DET_SCALE**) and an offset (**FF_DET_OFFSET**). In *Example 1* scale is defined for 8 detents, while *Example 2* shows scale defined for 6 detents. *Example 5* shows the use of offset to move detents in either direction. In addition, it is possible to limit which detents are active (**FF_DET_RANGE**), which is illustrated by *Example 3-5*.

LIMITED MOVEMENT RANGE

It is also possible to program a limited movement range (**FF_LIM_RANGE**) as shown by *Example 6*. This is applied separately and can be combined with all force feedback modes. It is also possible to define the force applied (**FF_LIM_SLOPE**) to counter movement beyond the programmed limits.

CUSTOM FORCE PROFILE

All examples show their corresponding force profile. This profile shows what data needs to be uploaded (**PROFILE_UPLOAD**) to the custom force profile to replicate the shown behavior. Each data point in the force profile specifies how much force should be applied when the slider is in that specific location.



DS PROTOTYP

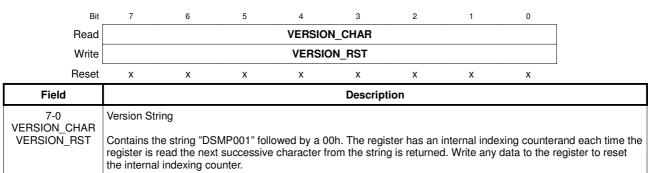
REGISTER LAYOUT

REGISTER	ADDRESS	FORMAT	RANGE	NOTES
VERSION	00h	8-bit		Read only, Streaming register ¹
PWM_LIMIT	10h	8-bit (unsigned)	0h-FFh	
PV_FILTER	11h	8-bit (unsigned)	0h-1Fh	
HAPTIC_KP	12h	8-bit (unsigned)	0h-FFh	
PID_KP	20h	8-bit (unsigned)	0h-FFh	
PID_KI	21h	8-bit (unsigned)	0h-FFh	
PID_KD	22h	8-bit (unsigned)	0h-FFh	
PID_BIAS	23h	8-bit (unsigned)	0h-FFh	
PID_DEADZONE	24h	16-bit (unsigned)	0h-1FFh	
PID_DEADZONE_TIME	26h	16-bit (unsigned)	0h-FFFFh	
PID_OVERLOAD_TIME	28h	16-bit (unsigned)	0h-FFFFh	
PID_FF_VELOCITY	30h	8-bit (unsigned)	0h-FFh	
PID_FF_ACCEL	31h	8-bit (unsigned)	0h-FFh	
PID_SETP_FILTER	32h	8-bit (unsigned)	0h-Fh	
MC_VELOCITY	40h	16-bit (unsigned)	0h-FFFFh	
MC_ACCEL	42h	16-bit (unsigned)	0h-FFFFh	
MC_SETTLE_MIN	44h	16-bit (unsigned)	0h-FFFh	
MC_SETTLE_MAX	46h	16-bit (unsigned)	0h-FFFh	
FF_MODE	50h	8-bit		
FF_DET_DZ	51h	8-bit (unsigned)	0h-FFh	
FF_DET_SLOPE	52h	8-bit (unsigned)	0h-FFh	
FF_DET_LEN	53h	8-bit (unsigned)	0h-FFh	
FF_DET_OFFSET	54h	16-bit (signed)	0h-FFFFh	
FF_DET_SCALE	56h	16-bit (unsigned)	0h-3FFFh	
FF_DET_RANGE	58h	16-bit		
FF_LIM_RANGE	5Ah	16-bit		
FF_LIM_SLOPE	5Bh	8-bit (unsigned)	0h-FFh	
FF_BRK_DRAG	5Dh	8-bit (unsigned)	0h-FFh	
FF_BRK_KP	5Eh	8-bit (unsigned)	0h-FFh	
SYSTEM	80h	8-bit		
STATE	81h	8-bit		
OUTPUT	82h	16-bit (signed)	FF00h-100h	Streaming register ¹
SETPOINT	84h	16-bit (unsigned)	0h-FFFh	Streaming register ¹
PV_FILTERED	8Ah	16-bit (unsigned)	0h-FFFh	Read only, streaming register ¹
PV	8Ch	16-bit (unsigned)	0h-FFFh	Read only, streaming register ¹
PID_ERROR	8Eh	16-bit (signed)	F001h-FFFh	Read only, streaming register ¹
MC_CMD	A0h	16-bit		Command, streaming register ¹
TF_CMD	A8h	8-bit		Command, streaming register ¹
PROFILE_SETUP	B1h	8-bit		Command register
PROFILE_UPLOAD	B2h	8-bit		Streaming register ¹
SCRATCH0	FCh	8-bit		
SCRATCH1	FDh	8-bit		
SCRATCH2	FEh	8-bit		
SCRATCH3	FFh	8-bit		

Note1 Streaming registers will not auto-increment the register pointer.

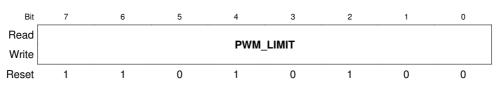
VERSION

Address: 00h



PWM_LIMIT

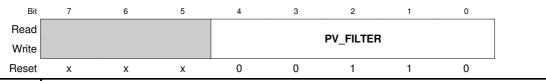
Address: 10h



Field	Description
7-0 PWM_LIMIT	Motor PWM drive limit Controls the maximum amount of power to the motor. For example, if the drive voltage is 12V setting this value to 127 (50%) vill limit the drive voltage to 6V.

PV_FILTER

Address: 11h



Field	Description
4-0 PV FILTER	The amount of filtering applied to the filtered PV register, PV_FILTERED.
	The filter is a single-pole low-pass filter with a sampling rate of 100kHz and a decay of 1-(1/(2 ^{PV_FILTER}))

HAPTIC_KP

Address: 12h

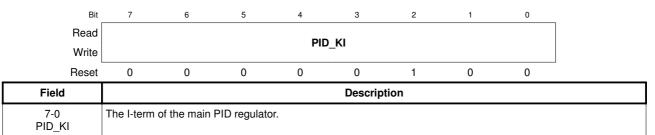
Bit	7	6	5	4	3	2	1	0	
Read					IC KP				
Write									
Reset	0	0	0	0	1	0	1	0	
Field					Descrip	tion			
7-0 HAPTIC_KP	The P-term	of the simpl	ified haptic	feedback P	regulator, us	ed when M	ODE = MOD	e_HF.	

PID_KP

Address: 20h 5 2 Bit 7 6 4 3 1 0 Read PID_KP Write Reset 0 0 0 1 1 1 1 1 Field Description 7-0 PID_KP The P-term of the main PID regulator.

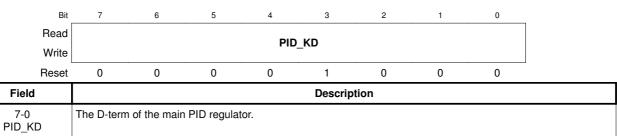
PID_KI

Address: 21h



PID_KD

Address: 22h



PID_BIAS

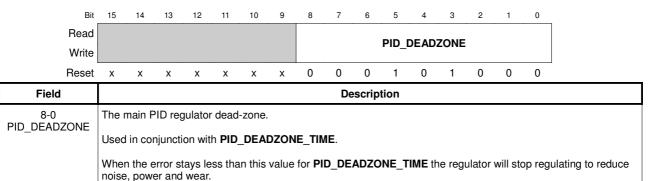
Address: 23h

Bit	7	6	5	4	3	2	1	0	
Read				PID_	BIAS				
Write Reset	0	0	0	0	0	0	0	0	
Field	0	0	0	0	Descript	-	0	0	
7-0 PID_BIAS								epresenting - account to asy	-50% to +50% o ymmetrical



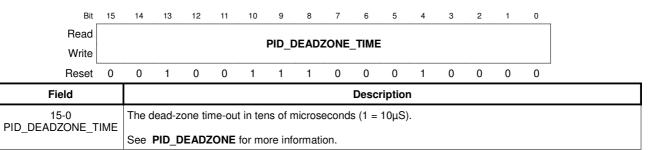
PID_DEADZONE

Address: 24h



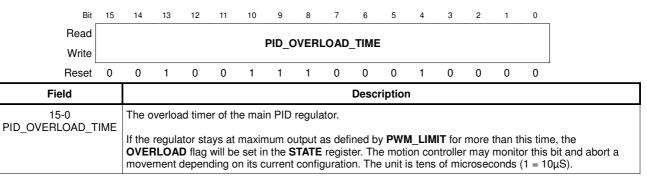
PID_DEADZONE_TIME

Address: 26h



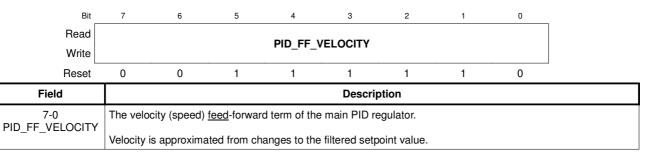
PID_OVERLOAD_TIME

Address: 28h



PID_FF_VELOCITY

Address: 30h



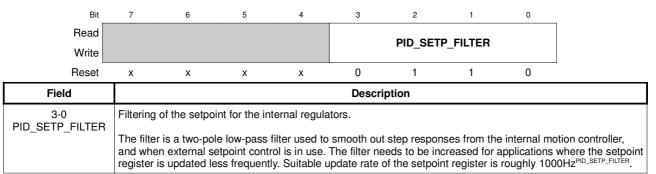
PID_FF_ACCEL

Address: 31h

Bit	7	6	5	4	3	2	1	0	
Read									
Write					_ACCEL				
Reset	0	0	0	0	0	1	0	0	
Field					Descrip	tion			
7-0	The accele	The acceleration feed-forward term of the main PID regulator.							
PID_FF_ACCEL	Acceleratio	n is approxi	nated from	changes to	the filtered s	etpoint value	<u>,</u>		

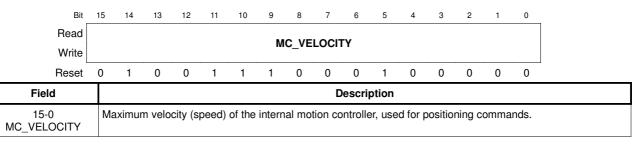
PID_SETP_FILTER

Address: 32h



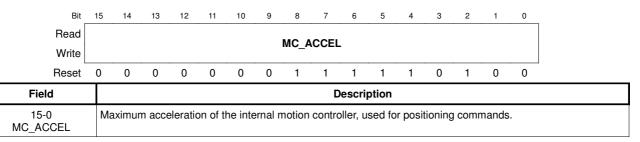
MC_VELOCITY

Address: 40h



MC_ACCEL

Address: 42h



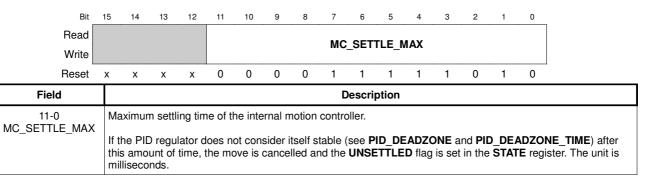
MC_SETTLE_MIN

Address: 44h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read									мс	SET	TLE I	MIN				
Write										_0						
Reset	Х	х	х	х	0	0	0	0	0	1	1	0	0	1	0	0
Field									D	escri	otion					
11-0	Mi	nimun	n settli	ng tim	e of th	ne inter	rnal m	otion	control	ler.						
MC_SETTLE_MIN	mo		the PI	D regu	ulator	then c	onside	ers itse	elf stab	le (se	e PID	_DEA	DZON	IE and		ettle at i DEAD

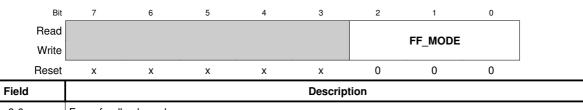
MC_SETTLE_MAX

Address: 46h



FF_MODE

Address: 50h



3-0 FF_MODE	Force feedback mode.
_	0b000 Disabled (FF DISABLE)
	0b001 Enabled - limits are active (FF_ENABLED)
	0b010 Brake mode (FF BRAKE)
	0b011 Custom profile (FF CUSTOM)
	0b100 Detents, soft (FF DETENT SOFT)
	0b101 Detents, sharp (FF_DETENT_SHARP)
	0b110 reserved
	0b111 Detents, custom profile (FF_DETENT_CUSTOM)



FF_DET_DZ

Address: 51h Bit 7 6 5 Read

Write				FF_D	ET_DZ							
Reset	0	0	1	1	0	0	0	0]			
Field					Descrip	tion						
7-0	Size of the	Size of the dead-zone / "bottom valley" of each detent.										
FF_DET_DZ	Used to define detent shape (when FF_MODE is any of FF_DETENT_n).											

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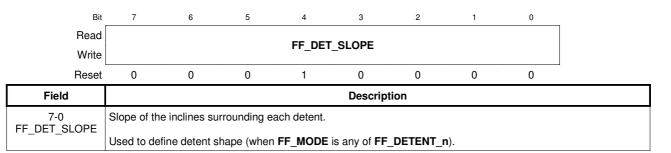
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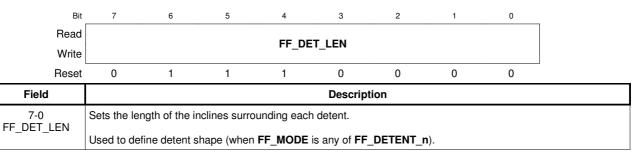
FF_DET_SLOPE

Address: 52h



FF_DET_LEN

Address: 53h



FF_DET_OFFSET

Address: 54h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read							EE	DET	0550	ст						
Write							гг <u>.</u>	_DET_								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Field									De	scrip	tion					
15-0 F DET OFFSET	Offse	t (mov	ve) det	tents (when	FF_M	ODE i	s any	of FF_	DETE	NT_n).				
						0h rep may be		ts mov ative.	/ing de	etents	by 1/1	6 th of	the ful	l scale	Э.	



FF_DET_SCALE

Address: 56h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read									DET	904						
Write										_304						
Reset	х	х	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Field									De	scrip	tion					
13-0 FF DET SCALE	Scale	e detei	nts (wl	nen FF	_MO	DE is a	any of	FF_D	ETEN	T_n).						
	As ar	n exan	nple, a	value	of 10	0h rep	resen	ts 16 (detent	s while	e a val	lue of	400h	repres	ents 4	deter

FF_DET_RANGE

Address: 58h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Read			DET	RAN	GE F	IRST					DET	RAN	GE L	AST			
Write					·												
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
Field									I	Descri	iption						
15-8 DET RANGE FIRS		Detent	range	– first	t deter	nt (whe	en FF_	_MOD	E is ar	ny of F	F_DE	TENT	_ n).				
		First de Each d 0, its ri	letent i	is split	into tv	<i>N</i> o pai	rts, ea	ch wit	h their	own c	letent	numb	er. The		detent	s left s	slope is numbered
		Detent	range	– last	deter	nt											
DET_RANGE_LAS		Last de See Di			,				0				be acti	ve.			

FF_LIM_RANGE

Address: 5Ah

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Read Write			LIM	I_RAN	IGE_L	.ow					LIM	_RAN	GE_H	ligh			
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
Field										Descr	iption						
15-8 LIM_RANGE_LOV		Limited If the u further	ser m	oves tl	he act	uator I	below	this li	— nit a f	orce d	efined	by FF	_LIM_	_SLOF			oplied to counter
7-0 LIM_RANGE_HIG		Limited If the u further	ser m	oves tl	he act	uator a	above	this li	— mit a f	orce d	efined	by FF	LIM	_SLOI			oplied to counter



FF_LIM_SLOPE

Address: 5Bh 5 Bit 7 6 4 3 2 0 1 Read FF_LIM_SLOPE Write Reset 0 0 0 0 0 0 0 0 Field Description 7-0 Limited movement range - slope (when FF_MODE is not FF_DISABLE). FF_LIM_SLOPE Sets the amount of force applied to counter movements beyond the limits specified in FF_LIM_RANGE.

FF_BRK_DRAG

Address: 5Dh

Bit	7	6	5	4	3	2	1	0
Read Write				FF_BR	K_DRAG			
Reset	0	0	1	0	0	0	0	0
Field					Descri	ption		
7-0 FF_BRK_DRAG		0	. –	IODE is FF _ d when tryin	_ BRAKE). g to move th	e actuator.		

FF_BRK_KP

Address: 5Eh

Bit	7	6	5	4	3	2	1	0
Read				FF_BF				
Write				гг_вг	IK_KF			
Reset	0	0	1	0	0	0	0	0
Field					Descri	iption		
7-0	Force b	orake – P ter	m (when FF	_MODE is F	F_BRAKE)			

FF_BRK_KP Sets the amount of force applied to counter movements the actuator.



SYSTEM

Address: 80h

Bit	7	6	5	4	3	2	1	0	
Read	RST		FACT	LOAD	SAVE	CALT		GCAE	
Write								GCAE	
Reset	х	x	х	х	х	х	х	0	
Field					Descri	iption			
7 RST	Write a	a one to this	bit to restart	the device.					
5 FACT		actory defaul bading factor	Ū		TATE will be	e reset and f	F_MODE w	ill be set to I	FF_NONE.
4 LOAD	If a val	onfiguration id configurat pading the co	ion does not	t exist in nor	n-volatile me		2		ded instead.
3 SAVE	Write a Once a To reve The no To preve second	ert a stored o on-volatile mo vent wear in	to store the on has been configuration emory has a a fault condi evice has be	current cont written to no back to def write endur ition the follo come active	figuration in a on-volatile m ault, issue a ance of 10.0 owing rules a , either from	emory it will write to SYS 00 cycles. upply: 1) The power-up of	be loaded a STEM with b configuration r a reset. 2)	oth SAVE an	on start-up. nd FACT set. e saved until one sfully storing a
2 CALT	In the	ate Touch Se event that the write a 1 to th	e touch sens					porting an inc	correct touch
0 GCAE		neral Call Ac this bit is set		-	the 00h gene	eral call addr	ress.		



STATE

Address: 81h

Bit	7	6	5	4	3	2	1	0
Read	INI	OVL	ABO	UNS	TACT	TOUCH	МС	DDE
Write	CINI	COVL	CABO	CUNS			мс	DDE
Reset							_	

Field	Description
7 INI/CINI	(Re-)initialized. This flag will always be set when the system is powered up, or after a reset, brown-out or other reason. Write a 1 to this location to clear the flag.
6 OVL/COVL	PID regulator overload. The PID regulatorhas detected an overload condition. See PID_OVERLOAD_TIME for more information. Write a 1 to this location to clear the flag.
5 ABO/CABO	Motion Controller Aborted. The motion controller has aborted a move due to overload or touch. Check OVL to determine the reason and see MC_CMD for more information on movements and error reporting. Write a 1 to this location to clear the flag.
4 UNS/CUNS	Motion Controller Unsettled. The motion controller finished while the PID regulator was unsettled. See PID_DEADZONE, MC_SETTLE and MC_CMD for more information. Write a 1 to this location to clear the flag.
3 TACT	Tactile event is in progress.
2 TOUCH	Actuator is being touched.
1-0 MODE	Current working mode. When writing the register, MODE will be ignored the written byte has any flags set – to prevent switching to idle when clearing flags. 0b00 Idle & force feedback modes (MODE_IDLE) 0b01 Haptic feedback P-regulation (MODE_HAPTIC) 0b10 PID regulation (MODE_PID) 0b11 PID+Motion Controller (MODE_PID_MC) Mode MODE PID MC is set automatically when issuing move commands and should never be set using this
	register. However, it is possible to abort the currently executing move by setting this register to something other than MODE_PID_MC while the move is in progress. When switching mode to MODE_PID from another mode the UNS and OVL flags will be cleared and SETPOINT will be loaded from PV. SETPOINT will also be loaded from PV when switching to MODE_HAPTIC from another mode.

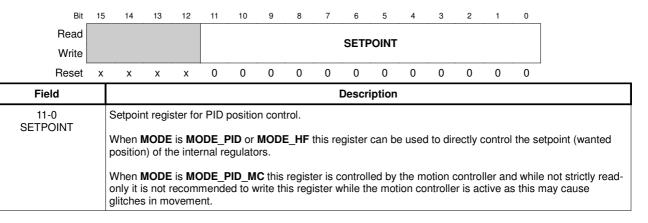


OUTPUT

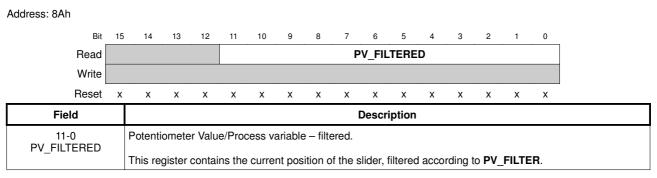
Address: 82h Bit Read OUTPUT Write Reset Field Description 15-0 Motor output register (torque). OUTPUT When MODE is MODE_IDLE and FFMODE is FF_DISABLED this register can be used to control motor torque directly. In all other configurations this register is read-only and contains the currently applied motor torque. The range is -256 to +256.

SETPOINT

Address: 84h

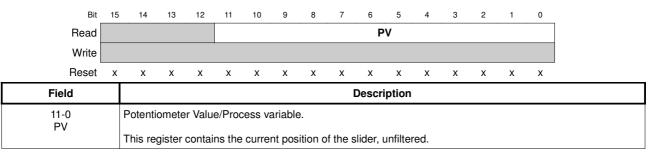


PV_FILTERED



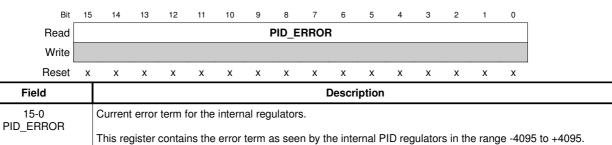
PV

Address: 8Ch



PID_ERROR

Address: 8Eh





MC_CMD

Address: A0h

1000.71011																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	_		
Read	MCA	OVL	АВО	UNS					F	V_FIL	TERE	D							
Write	ATO	AOV								MOVE	_СМІ	D							
Reset	х	х	х	х	х	х	х	х	х	х	х	х	х	х	х	х			
Field										Descr	iption	1							
15 ATO	A	Abort o	n touc	:h.															
	Т	The iss	ued m	iove w	ill be	aborte	d if th	e actu	ator is	touch	ied.								
14 AOV		Abort o														_			
		The iss PID_O								ator reg	gisters	s an ov	erload	d conc	lition.	See			
11-0 MOVE CMD	N	Novem	ient co	mmar	nd.														
_	N te a	NOVE_ o its or	_CMD riginal C_ACC	. MÕD state o CELEF	E will once t RATIO	be sw he mo N . It is	vitchec ove ha s poss	to M s com	ODE_ pleted	PID_N I. The anoth	IC for move ner mo	the du will ad ove cor	iration Ihere t mman	of the o con d while	e move straint e the f	ement s set k	sition spe and swite by MC_VI still being	ched bac ELOCIT	:k
15 MCA	N	Notion	Contr	oller A	ctive.	_													

This flag will be set for the duration of the motion controller activation and will clear automatically when the movement is completed. This flag is defined by **MODE** = **MODE_PID_MC**.

TF	CMD

14 OVL

13 ABO

12 UNS

11-10

PV_FILTERED

See STATE - OVL.

See STATE - ABO.

See STATE - UNS.

See PV_FILTERED.

Address: A8h

Bit	7	6	5	4	3	2	1	0			
Read		TF_TIMER									
Write	TF_STRENGTH			TF_S	PEED	TFNTF	TF_DU	RATION			
Reset	x	х	х	х	х	х	х	x			
Field		Description									
7-5 TF_STRENGTH	Used to	Used to trigger a tactile feedback event.									
	Sets the	Sets the strength of the event, a value of 0 will cancel any currently active event.									
4-3 TF_SPEED	Sets the	Sets the vibration speed of the event.									
2 TFNTF	Force t	Force the event, even if the controller is not being touched.									
1-0 TF_DURATION	Sets the	Sets the duration of the event.									
7-0 TF_TIMER		If a tactile feedback event is in progress this register contains the internal counter, counting down until the end of the event. Will return 0 when no tactile feedback event is in progress.									

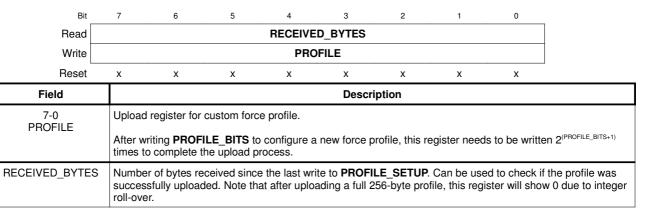


PROFILE_SETUP

Address: B1h											
Bit	7	6	5	4	3	2	1	0			
Read Write						P	ROFILE_BIT	rs			
Reset	0	0	0	0	0	0	0	0			
Field		Description									
2-0 PROFILE_BITS	When the After with Once the After with Once the After with Once the After with Once the After A	his register i riting this fie his has beer	ld, write 2 ^{(PR} 1 done it will	vill clear the ^{IOFILE_BITS+1)} by be possible	currently upl tes to PROF to use force DE appropria	ILE_UPLO	AD to upload	d the new fo			

PROFILE_UPLOAD

Address: B2h



SCRATCHn,

Address: FCh-FFh

